

Maximizing process efficiency with dual current exposure strategy

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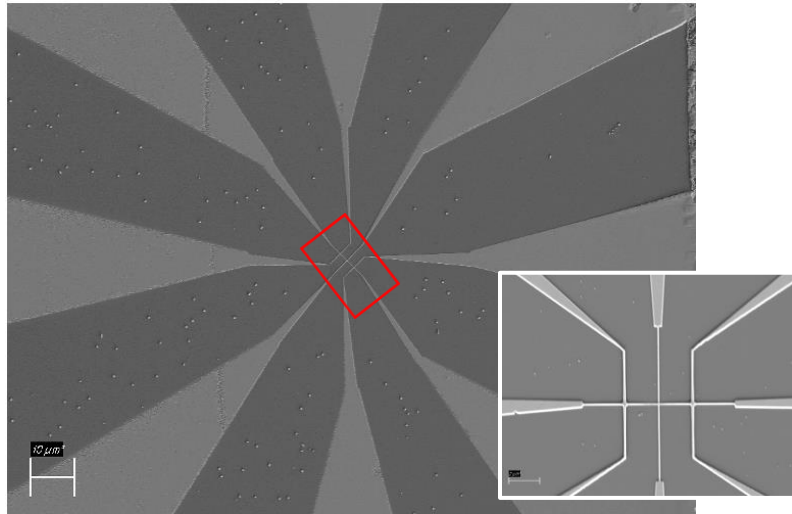


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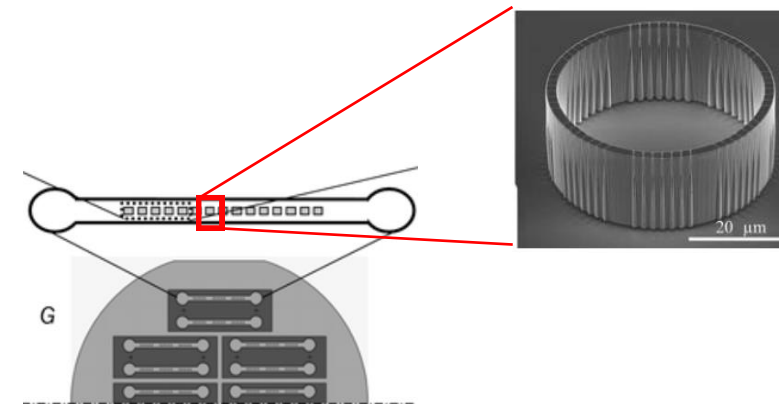
Fabrication of continuous, multiscale pattern (whether etched or metalized) can be lengthy, tedious

Example 1: nanowires and PADS



Fabrication process:
 EBL pattern nanowire (20-60nm width)
 Metal deposition + lift off
 Photolithography to pattern bigger pads (~100μm)
 Metal deposition + lift off

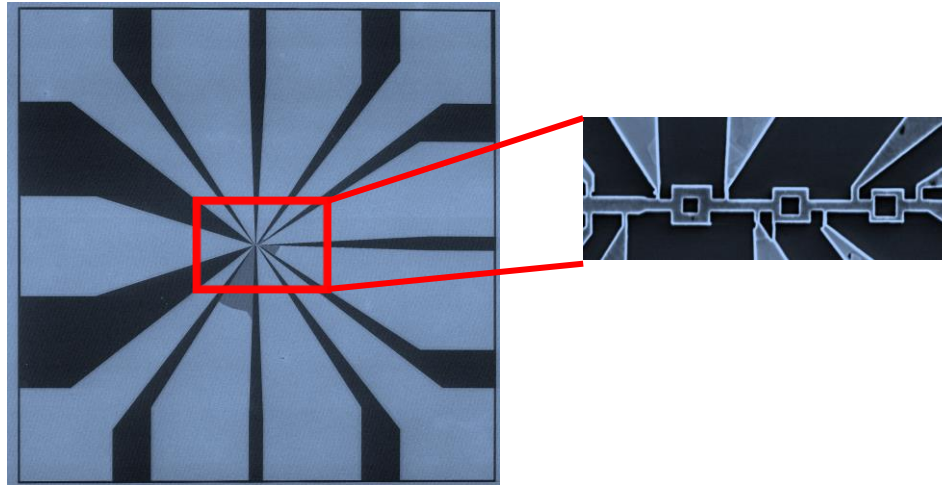
Example 2: microbioreactor within microfluidic channel



Fabrication process:
 EBL pattern bioreactor, with 200nm slits
 Metal deposition + lift off
 Photolithography to pattern microfluidic channel
 Etch both bioreactor and microfluidic channel together

We have an electron beam lithography system that allows dual current exposure

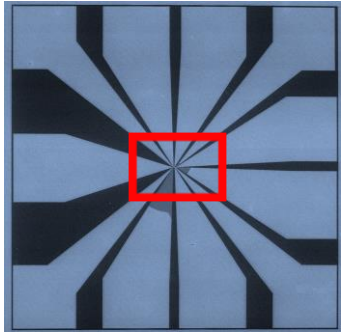
Simple device example fabricated using dual current exposure :



Larger features up to $500\mu\text{m}$, smaller feature $200\text{-}300\text{nm}$

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Simple device example fabricated using dual current exposure :



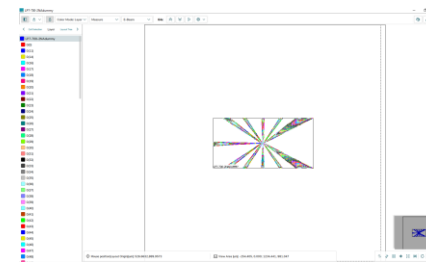
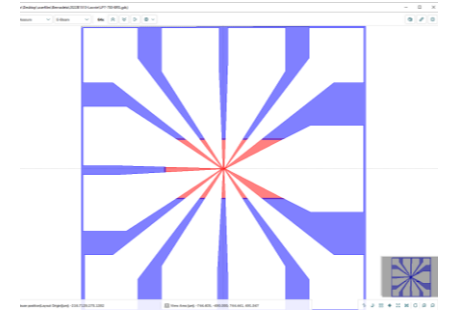
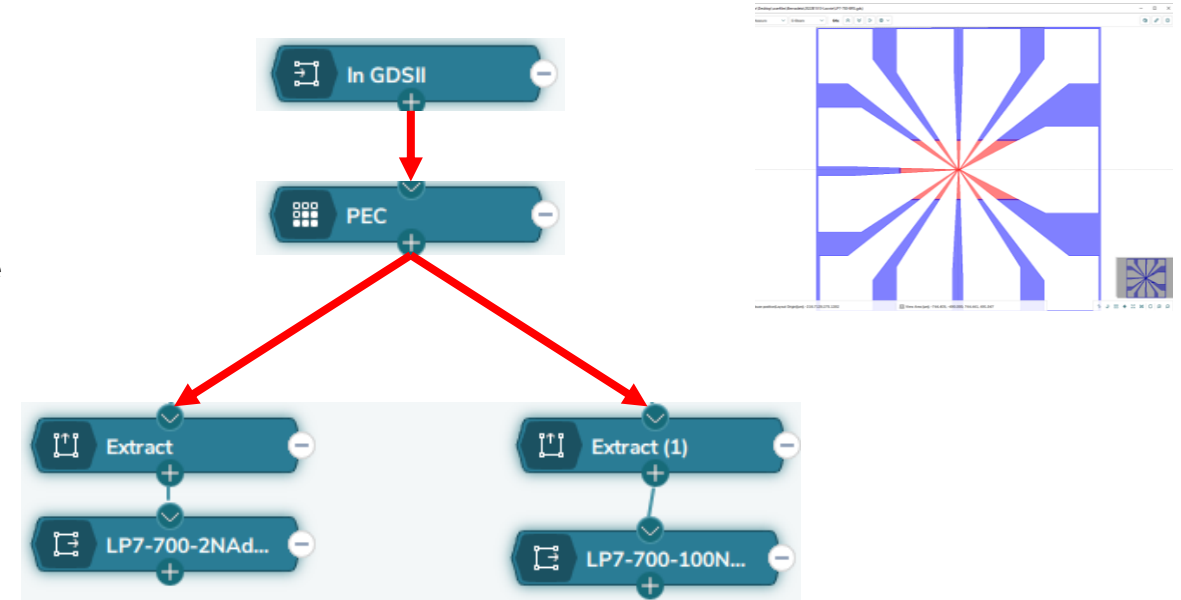
1. Layout preparation

- Select the cutoff feature size to be exposed at lower current vs at higher current
- Separate them into two layers.
- Draw some overlap layout where the two layers meet

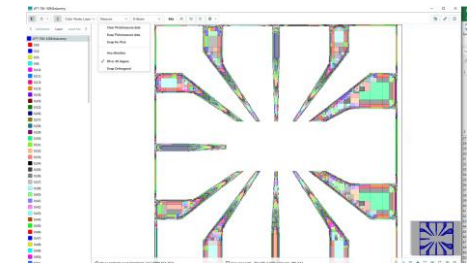
2. Import gds

3. Run PEC before exporting the layout into two v30's

4. Extract, Heal, and Export

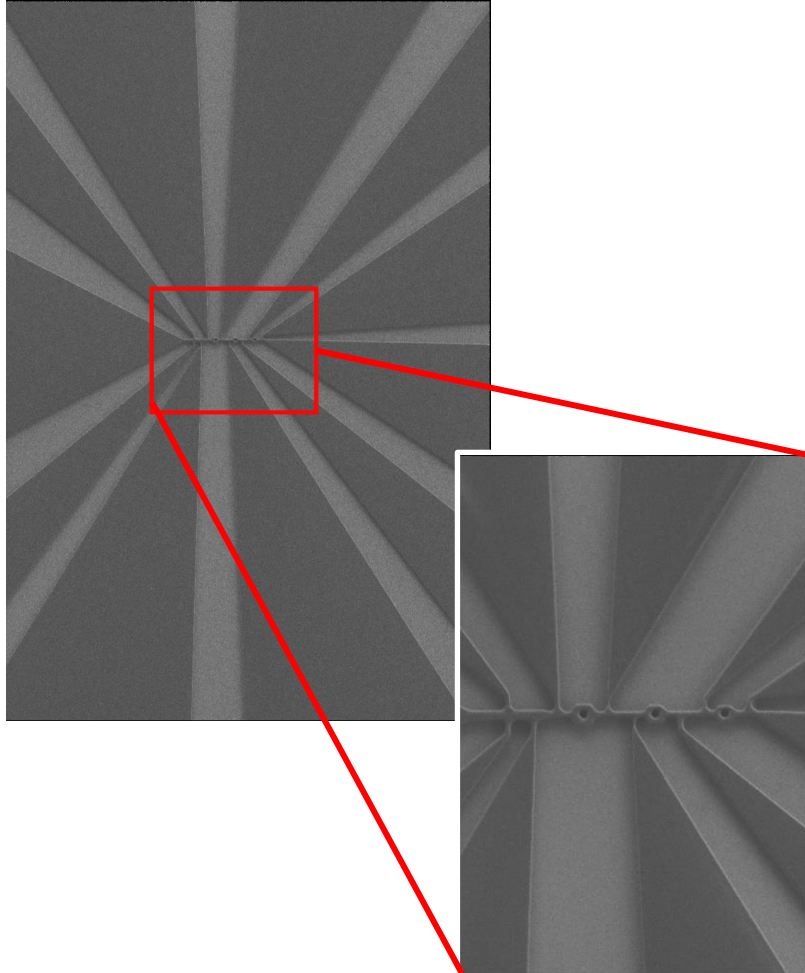


v30 for lower current exposure (e.g. 1nA, 2nA)



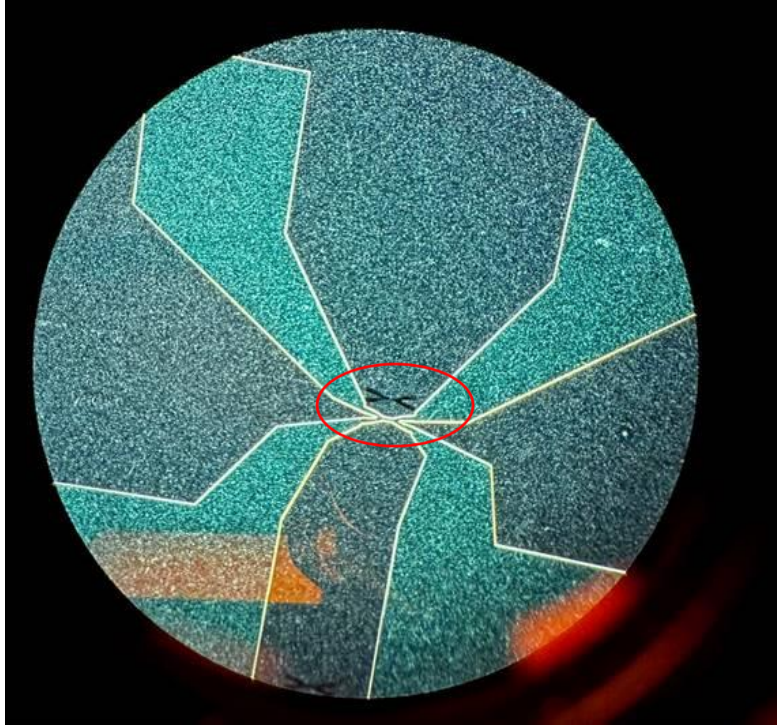
v30 for higher current exposure (e.g. 40nA, 100nA)

SEM imaging of the exposure result:



Placing PEC before instead of after splitting the layers reduces/minimizes proximity effect of higher current exposure on smaller features.

There is still some challenge with offset in dual current exposure: patterns of two currents did not align properly, i.e., there is offset.



The offset is due to the (bounding box) of two layers do not share the same center location.

We fixed it by adding a very small feature (e.g., square) on four corners at the same position for both layers.

We are very interested if Beamer has a solution for this offset.

Dual current exposure save extra process steps and exposure time

Exposure time :

1. For 3x3 array of the device example on a 5-10 mm chip size:
 - Exposure only at 2nA current took 5-6 hours.
 - Dual current exposure (2nA and 100nA) took 1-2 hours
2. Exposure time saving is more significant when exposure is performed on 4" wafer.
We had a pattern ranging from 20nm dots to several μm feature size, arrayed on 4" wafer.
 - Exposure only at 2nA current : ~158 hours
 - Dual current exposure (2nA and 40nA) : ~8 hours
 - Dual current exposure (2nA and 100nA) : ~4.5 hours

Process step:

Only requires one lithography step, one deposition step

- the dual current exposure does not require alignment mark !

Thank you!

Questions?
Comments?